CLAIMS

I claim:

1. A system for determining timing in an electrical circuit comprising:
    a. a netlist input for receiving a circuit netlist representing the topology of the electrical circuit to be timed;
    b. an assertion input for receiving a set of one or more assertions representing boundary timing conditions;
    c. a delay variability input for receiving a list of one or more sources of delay variation that contain variability information of one or more of the sources of variation;
    d. a model input for receiving a parameterized delay model, the parameterized delay model containing one or more models for a delay of one or more components of the electrical circuit, each model being a function of one or more of the sources of delay variation; and
    e. a process that determines and outputs a statistical arrival time of one or more nodes of the electrical circuit, the statistical arrival time being in the form of a weighted sum of probability distributions of one or more of the sources of variation.

2. A system, as in claim 1, where the process determines the statistical arrival times by visiting each node of the electrical circuit only once.

3. A system, as in claim 1, where the system further determines and outputs a statistical required arrival time of one or more nodes of the electrical circuit, the statistical required arrival time being in the form of a weighted sum of probability distributions of one or more of the sources of variation.

4. A system, as in claim 1, where the process determines and outputs a statistical slack of one or more nodes of the electrical circuits, the statistical slack being in the form of a weighted sum of probability distributions of one or more of the sources of variation.

5. A system, as in claim 1, where the process determines and outputs a statistical slew of one or more nodes of the electrical circuits, the statistical slew being in the form of a weighted sum of probability distributions of one or more of the sources of variation.

6. A system, as in claim 1, where the process performs a late mode statistical timing analysis and outputs late mode arrival times.

7. A system, as in claim 1, where the process performs an early mode statistical timing analysis and outputs one or more early mode arrival times.

8. A system, as in claim 1, where one or more separate rising and falling statistical delays are provided for each component of the electrical circuit and the process

determines and outputs one or more separate rising and falling statistical arrival times for one or more nodes of the electrical circuit.

9. A system, as in claim 8, where the process determines and outputs one or more of the separate rising and falling statistical required arrival times, one or more separate rising and falling statistical slacks, and one or more separate rising and falling statistical slews for one or more nodes of the electrical circuit.

10. A system, as in claim 1, where the electrical circuit is one or more of the following: a combinational circuit, a sequential circuit, a static logic circuit, and a dynamic logic circuit.

11. A system, as in claim 1, where the electrical circuit is a sequential circuit that contains one or more of the following: an edge-triggered latch, a master-slave latch, a level-sensitive latch, and a transparent latch.

12. A system, as in claim 1, where the circuit contains multiple clock phases.

13. A system, as in claim 1, where the parameterized delay model for each component of the electrical circuit comprises one or more of: a deterministic part, a correlated part, and an independently random part.

14. A system, as in claim 13, where the sources of variation are correlated.

15. A system, as in claim 13, where the sources of variation are independent.

16. A system, as in claim 1, where the parameterized delay models are pre-stored in a table in one or more memories of the system.

17. A system, as in claim 1, where the parameterized delay models are pre-stored as coefficients of delay equations in one or more memories of the system.

18. A system, as in claim 1, where the parameterized delay models are determined by circuit simulation on-the-fly.

19. A system, as in claim 1, where each assertion is one of deterministic and statistical.

20. A system, as in claim 1, where clock-edge information is one of deterministic and statistical.

21. A system, as in claim 1, where the electrical circuit is a sequential circuit and a guard time of each timing test is one of deterministic and statistical.

22. A method for analyzing timing of an electrical circuit, comprising the steps of:

a. inputting a netlist, one or more assertions, one or more parameterized delay models and one or more sources of variation;

b. building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. levelizing the graph for forward propagation of statistical arrival times; and

d. at each level of the timing graph, propagating one or more statistical arrival times at each of the nodes, each of the statistical arrival times being a weighted sum of probability distributions of one or more of the sources of variation.

23. A method, as in claim 22, where the statistical arrival times are determined by visiting each node of the electrical circuit only once.

24. A method, as in claim 22, where the statistical slew of one or more nodes of the electrical circuits is determined and outputted, the statistical slew being in the form of a weighted sum of probability distributions of one or more of the sources of variation.

25. A method, as in claim 22, where a late mode statistical timing analysis is performed.

26. A method, as in claim 22, where an early mode statistical timing analysis is performed.

27. A method, as in claim 22, where separate rising and falling statistical delays are provided for each component of the electrical circuit and separate rising and falling statistical arrival times are determined for one or more nodes of the electrical circuit.

28. A method, as in claim 27, where one or more of separate rising and falling statistical required arrival times, separate rising and falling statistical slacks and separate rising and falling statistical slews are determined at one or more nodes of the electrical circuit.

29. A method, as in claim 22, where the electrical circuit is one or more of the following: combinational, sequential, static logic, and dynamic logic.

30. A method, as in claim 22, where the electrical circuit is a sequential circuit that contains one or more of the following: edge-triggered latches, master-slave latches, level-sensitive latches, and transparent latches.

31. A method, as in claim 30, where the guard time of each timing test is one of deterministic and statistical.

32. A method, as in claim 22, where the circuit contains multiple clock phases.

33. A method, as in claim 22, where the parameterized delay model for each component of the electrical circuit comprises one or more of: a deterministic part, a correlated part, and an independently random part.

34. A method, as in claim 33, where the sources of variation are correlated.

35. A method, as in claim 33, where the sources of variation are independent.

36. A method, as in claim 22, where the parameterized delay models are pre-stored in a table.

37. A method, as in claim 22, where the parameterized delay models are pre-stored as coefficients of delay equations.

38. A method, as in claim 22, where the parameterized delay models are determined by circuit simulation on-the-fly.

39. A method, as in claim 22, where each assertion is one of deterministic and statistical.

40. A method, as in claim 22, where clock-edge information is one of deterministic and statistical.

41. A method, as in claim 22, further comprising the steps of :

a. levelizing the graph for backward propagation of statistical required arrival times; and

b. at each level of the timing graph, propagating one or more statistical required arrival times at each of the nodes, each of the statistical required arrival times being a weighted sum of probability distributions of one or more of the sources of variation.

42. A method, as in claim 41, where the statistical required arrival times are determined by visiting each node of the electrical circuit only once.

43. A method, as in claim 41, where the statistical slack of one or more nodes of the electrical circuits are determined and outputted, the statistical slacks being in the form of weighted sums of probability distributions of one or more of the sources of variation.

44. A system for analyzing timing of an electrical circuit, comprising:

a. means for reading the netlist, assertions, parameterized delay models and list of sources of variation;

b. means for building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. means for levelizing the graph for forward propagation of statistical arrival times; and

d. at each level of the timing graph, means for propagating one or more statistical arrival times at each of the nodes, each of the statistical arrival times being a weighted sum of probability distributions of one or more of the sources of variation.

45. A system, as in claim 44, further comprising the steps of :

a. means for levelizing the graph for backward propagation of statistical required arrival times; and

b. at each level of the timing graph, means for propagating one or more statistical required arrival times at each of the nodes, each of the statistical required arrival times being a weighted sum of probability distributions of one or more of the sources of variation.

46. A computer memory storing a method for analyzing timing of an electrical circuit, the method comprising the steps of:

a. inputting a netlist, one or more assertions, one or more parameterized delay models and one or more sources of variation;

b. building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. levelizing the graph for forward propagation of statistical arrival times; and

d. at each level of the timing graph, propagating one or more statistical arrival times at each of the nodes, each of the statistical arrival times being a weighted sum of probability distributions of one or more of the sources of variation.

47. A computer memory, as in claim 46, where the method further comprises the steps of :

a. levelizing the graph for backward propagation of statistical required arrival times; and

b. at each level of the timing graph, propagating one or more statistical required arrival times at each of the nodes, each of the statistical required arrival times being a weighted sum of probability distributions of one one more of the sources of variation.

48. A computer output product produced by the process of analyzing timing of an electrical circuit, the process comprising the steps of:

a. inputting a netlist, one or more assertions, one or more parameterized delay models and one or more sources of variation;

b. building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. levelizing the graph for forward propagation of statistical arrival times; and

d. at each level of the timing graph, propagating one or more statistical arrival times at each of the nodes, each of the statistical arrival times being a weighted sum of probability distributions of one or more of the sources of variation.

49. A computer output product, as in claim 48, where the method further comprises the steps of :

a. levelizing the graph for backward propagation of statistical required arrival times; and

b. at each level of the timing graph, propagating one or more statistical required arrival times at each of the nodes, each of the statistical required arrival times being a weighted sum of probability distributions of one or more of the sources of variation.